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ADTST.031AUS PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Hiroaki Yamoto et al.	Group Art Unit 2123
Serial No.	:	09/941,396	
Filed	:	August 28, 2001	
For	:	METHOD FOR DESIGN VALIDATION OF COMPLEX IC	
Examiner	:	Unknown	

PRELIMINARY AMENDMENT

Hon. Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

This is a preliminary amendment for the above-identified patent application. Please make the following changes:

IN THE SPECIFICATION:

(1) The following paragraph has been inserted between line 1 and line 2 in Page 1:

This application claims the benefit of Provisional Patent Application No. 60/237,001 filed September 29, 2000.

(2) The paragraph from page 16, line 21 to page 16, line 30 has been replaced with the following:

The event based test system (design test station DTS) 82 includes a VCD compiler 218, an event viewer 222, and a VCD writer 220. The VCD compiler 218 translates the VCD data to event data for use by the event based test system 82. The event viewer 222 and the VCD writer 220 correspond to the VCD